REMARKS

This amendment is filed in response to the Office Action mailed on July 14, 2004. All objections and rejections are respectfully traversed.

Claims 1-48 are in the case.

Claims 9 and 20 were amended to better claim the invention.

Claims 22-48 were added to better claim the invention.

At Paragraphs 1 - 10 Claims 1, 2, 4-7, 11-16, 18, and 21 were rejected under 35 U.S.C. 102(e) as being anticipated by Wu U. S. Patent No. 6,151,644 issued on November 21, 2000 (hereinafter Wu).

The present invention, as set forth in representative claim 1, comprises in part:

> 1. A method for ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers***, the method comprising the steps of:
>
> ***including a context memory in each pipeline row;***
>
> organizing the context memory as a plurality of window buffers of a defined size;
>
> apportioning each packet into contexts corresponding to the defined size associated with each window buffer; and

correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out of order issues involving the contexts of the packet.

Wu discloses a dynamically configurable buffer for a device for a computer network. Wu's buffer is first configured for a large size "packet buffer", and also is configured with a packet buffer divided into smaller pieces referred to as a "packet cell". A large packet is stored in a "packet buffer", and a small packet may be stored in a "packet cell" if the packet is small enough. The packet cell size can be increased dynamically to accommodate different size packets.

Applicant respectfully urges that Wu has no disclosure of Applicant's claimed novel ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers***. Particularly, Wu has no disclosure of Applicant's claimed ***plurality of processors arrayed as pipeline rows and columns***.

Also, Applicant respectfully urges that Wu has no disclosure of Applicant's claimed novel ***including a context memory in each pipeline row***. Firstly, Wu has no disclosure of Applicant's claimed ***each pipeline row***. Secondly Wu has no disclosure of Applicant's claimed novel ***including a context memory*** in his design. Further, Wu has

no disclosure of ***including a context memory in each pipeline row***, especially since Wu has no disclosure of a ***pipeline row***.

Accordingly, Applicant respectfully urges that Wu is legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. § 102 because of the absence from Wu of Applicants claimed novel ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers***; and there is absent from Wu Applicant's claimed novel ***plurality of processors arrayed as pipeline rows and columns***.

At Paragraph 11 - 16 of the Office Action claims 3, 8, 17, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Sindhu.

Applicant respectfully notes that claims 3, 8, 17, and 19 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, claims 3, 8, 17, and 19 are believed to be in condition for allowance.

All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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